WHAT IS CLAIMED IS:

1. In a system in which reconfigurable compute engines have input and output pins and are interconnected to perform a predetermined function and in which each of said reconfigurable compute engine includes an application layer and a physical layer, an interconnect fabric, comprising:

a reconfigurable interconnect layer between said application layer and said physical layer for defining the identity and function of said input and output pins so as to effectuate the interconnection of said reconfigurable compute engines to perform said predetermined function.

2. The interconnect fabric of Claim 1, wherein pairs of said engines are complementary.

3. The interconnect fabric of Claim 2, wherein said pairs of engines have complementary pins.

4. The interconnect fabric of Claim 3, wherein said complementary pins include pins having transmitting and receiving functions respectively.

5. The interconnect fabric of Claim 3, wherein said complementary pins function to transmit timing signals therebetween.

6. The interconnect fabric of Claim 3, wherein said timing signals include a strobe.

7. The interconnect fabric of Claim 3, wherein one of said pins supports the transmission of packet switched signals.

8. The interconnect fabric of Claim 3, wherein one of said pins supports the transmission of circuit switched signals.

9. The interconnect fabric of Claim 3, wherein one of said pins supports discrete signal level transmissions.

10. The interconnect fabric of Claim 1, wherein said predetermined function includes spatial processing.

11. The interconnect fabric of Claim 1, wherein said predetermined function includes communications.

12. The interconnect fabric of Claim 1, wherein said predetermined function includes signal intelligence.

13. The interconnect fabric of Claim 1, wherein said predetermined function includes jamming.

14. The method of Claim 1, wherein one of said engines includes a field programmable gate array.

15. A method for rapidly switching the mode of operation of a system employing a number of reconfigurable compute engines having existing interconnection physical layers and application layers, comprising the steps of:

interconnecting selected reconfigurable compute engines by providing a reconfigurable interconnect layer between the application layer and the physical layer of a reconfigurable compute engine for changing the identity and functions of the inputs to and outputs of the engine so as to tailor the inputs and outputs to use the existing physical layer in running the corresponding application, whereby a mode change can be made by loading a new application in an engine and reconfiguring the interconnect layer to accommodate the new application using the existing physical layer.

16. The method of Claim 15, wherein the inputs and outputs occur at pins selected by the reconfigurable interconnect layer.

17. The method of Claim 16, wherein interconnected engines have complementary pins.

18. The method of Claim 16, wherein the functions of the inputs and outputs are selected from the group consisting of a packet switched data transfer function, a circuit switched data transfer function and a discrete signal level transfer function.